Broad-Band Microwave Class-C Transistor Amplifiers

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Abstract—**Useful techniques for large-signal transistor characterization and the design of broad-band input- and output-matching structures are described. The techniques are particularly oriented to computer-aided design. Useful topologies for realizing broad-band matching networks are provided. Measured performance data for a 13-W, 1010- to 1460-MHz stage are included. An assessment of broad-band utilization of two circuits is graphically undertaken in conjunction with the Bode constant-resistance integral theorem.**

Introduction

THE current emphasis upon broad-band transmitters for communications, radars, and electronic countermeasures presents many design challenges to the microwave engineer. The techniques stemming from traditional narrow-band circuit design, often usable for realizing 50- to 100-MHz bandwidths, are inadequate for broader frequency ranges.

Optimal seeking programs are an indispensable aid for large-signal broad-band design. If success is to be assured, the microwave designer must have a conceptual understanding of promising circuit topologies. Meaningful design constraints must be established so that the optimal design can be selected from thousands of possible designs. Unless the transistor itself can be fully simulated in the program, one requires a description of what the transistor desires for input and output loading in terms of some defined circuit quantities. This might take the form of describing an acceptable driving-point impedance as a function of frequency, together with permissible deviations from the specific values. Establishing design constraints for the computer search ordinarily presents the most difficulty.

Large-Signal Transistor Characterization

Broad-band large-signal microwave-amplifier design is considerably more complicated than small-signal design.[1] Bandwidth for small-signal stages would generally be specified as the frequency range over which the gain is maintained within some specified deviation from a nominal value. In small-signal design, input- and output-matching circuits could be varied mutually to meet an acceptable gain and bandwidth, while well-defined stability boundaries are assured. In large-signal stages, the output-matching circuit must principally satisfy good collector efficiency and adequate saturated output power with good stability over the operating bandwidth. While the output match also affects power gain, this factor is usually in conflict with the principal objective of saturated output power. Consequently, power gain often must be sacrificed from 1 to 2 dB from the maximum usable value. The input-matching circuit design is principally concerned with power-gain conservation and gain flatness. The design of the input circuit has no relationship to saturated output power and collector efficiency.

With large-signal class-C microwave stages, complete equivalent-circuit representations which account for forward and reverse power flows are not available. Similarly, transistor characterization that would serve large-signal objectives as effectively as S-parameter characterization serves small class-A design is not widely available. Where complete large-signal characterization has been undertaken, a large number of painstaking measurements have been necessary.

In recent years, there has been considerable discussion concerning appropriate large-signal characterization for microwave transistors. The dialogue often shifts to considerations and difficulties in measuring large-signal S-parameters, particularly s_{12} and s_{21}, for transistors in class-C operation. These measurements would be very involved. If one could assume complete S-parameter characterization to be available, a new dilemma would present itself. While S-parameter characterization is excellent for assuring stability and level power gain in broad-band designs, there are no meaningful means for S-parameter consideration of the two vital large-signal design factors, saturated output power capability and collector efficiency.[2] These two factors are a function of the collector load-line impedance. S-parameter characterization would only permit relating the load line to the output impedance of the transistor in terms of power gain and stability of the amplifier. This should not be interpreted as a condemnation of S-parameters in every instance of large-signal design, but rather to indicate that they do not offer the characterization information necessary for assuring some objective minimum output power and minimum collector efficiency in the design.

Transistor manufacturers offer some collector loading information for power transistors on transistor data sheets. These impedance data are given for rated output power over the normal frequency range of application for the particular transistor. There are several vague points in such data. 1) At what point on the collector lead is such data referenced? 2) When the real component of impedance is low (often the 2- to 5-Ω level), one is concerned that losses which arise in the tuning stubs or other matching elements may be obscuring the measured impedance data. 3) Often one wishes for data at other frequencies, output power levels, and supply voltages. 4) How does one stipulate permissible deviations from the specific impedance so that acceptable efficiency and power output can be assured? This is an important consideration, since there will be no realizable broad-band circuit design that can present the optimum loading over the entire frequency band.

Belohoubek *et al.* [1]–[3] have established a complete

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[1] This is acknowledged to be an oversimplification in small-signal designing where noise figures and 1-dB compression levels are included in the objective.

[2] There are many definitions for operating efficiency. Collector efficiency in this paper will be defined to mean the ratio of RF output power to dc collector input power.

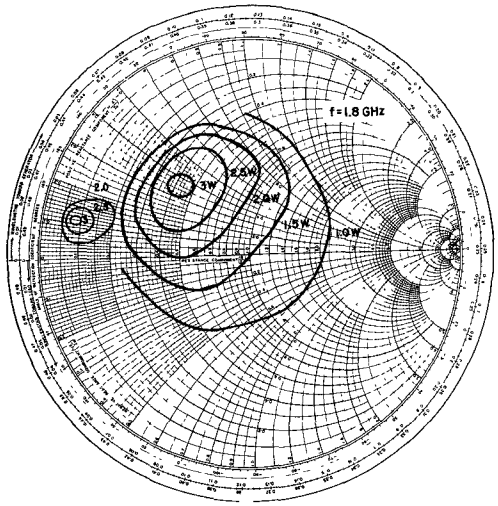

Fig. 1. Load-pull data for a transistor stage at 1.8 GHz showing contours of constant power as a function of impedance.

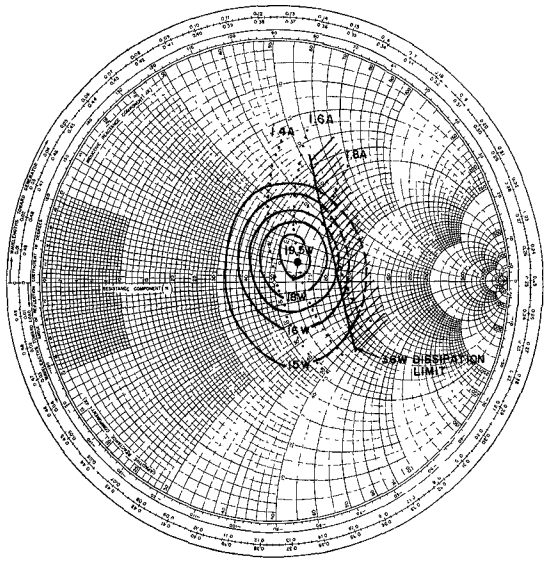

Fig. 2. Load-pull data at 1.5 GHz illustrating contours of constant output power and constant dc collector current as a function of load impedance. $V_{dc}=28$ V. $T_C=30°C$. $P_{in}=3$ W. $f=1.5$ GHz.

large-signal collector load-line characterization method known as load-pull measurement which interrelates the power output, collector efficiency, power gain, and stability for class-C amplifiers. The characterization has similarities with the Rieke[4] characterization for klystrons. The load-pull measurement method consists of operating the transistor at some specific input drive power, collector supply voltage, and frequency while monitoring the output power, dc collector current, and stability as functions of precisely established collector load-line impedances. The data are taken at a sufficient number of frequencies over the band of interest for broad-band characterization. The data are ideally applied to the computer-aided design of output-matching networks.

The measurements are manually made using an ultraprecision calibrated slug tuner for presenting the range of load impedances desired. The procedure is time-consuming for thorough characterization which requires measurements at perhaps 30–50 collector impedances at each frequency. The potential of this technique should ultimately justify the development of a semiautomated load-pull system which would make microwave large-signal characterization almost as straightforward as the automatic network analyzers have made S-parameter characterization of small-signal microwave transistors.

Figs. 1 and 2 illustrate typical load-pull characterization data presented in Smith chart form. (These data are furnished through the courtesy of E. Belohoubek.) Fig. 1 illustrates a family of constant power-output loci for a transistor stage operating under constant input drive at 1.8 GHz. The larger family of isopower contours relates power output to terminating impedances following the transistor output-matching network. The smaller family of contours relates to load-line impedances presented at the collector node on the transistor chip. Fig. 2 shows contours of constant power and constant dc collector current as a function of terminating impedances outside a complete transistor stage under constant drive at 1.5 GHz.

The load-pull system, if automated, could readily permit practical extension of transistor characterization data to include several input drive levels, supply voltages, and heat-sink temperatures. With such data available, enhanced optimal broad-band designs could be pursued using computer-aided techniques. Furthermore, performance sensitivity of an amplifier could be considered in view of such realities as VSWR variations in load terminations.

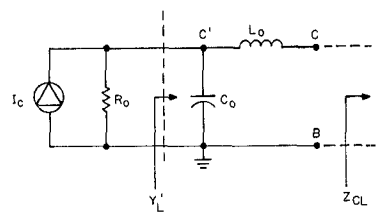

Fig. 3. A large-signal common-base transistor-output equivalent circuit.

While load-pull transistor measurements represent the ultimate characterization method for large-signal stage design, unfortunately it is not available to most designers. A broad-band design procedure has been conceived [5] based on a first-order approximation to an output equivalent circuit for large-signal transistors. The systematic procedure has repeatedly afforded excellent broad-band performance for class-C microwave-transistor stages.

The large-signal equivalent output circuit for a common-base transistor is depicted in Fig. 3. Points C and B designate the conventional collector and grounded-base terminals external to the transistor package. The collector series-lead inductance is represented by L_o. For most microwave transistor packages, this would typically have a minimum value of between 0.6 and 1.0 nH. In some instances, this minimum series-load inductance will limit the broad-banding potential of a transistor. The effective large-signal output capacitance of the transistor is represented by C_o. Experience with over 20 different microwave transistors has repeatedly confirmed that the value of C_o is best represented by measuring C_{cb} of the packaged transistor with collector-to-base junction reverse biased at the collector supply voltage V_{cc}. This measurement is made on a capacitance bridge at 1 MHz. Initially, it was anticipated that transistor large-signal swings would be likely

to cause the value of C_o to be 20–30 percent greater than the value measured at V_{cc}; however, carefully relating the effective large-signal capacitance to load-pull and other data has confirmed the value of C_o as stated. The explanation for this observed relationship is not known.

The output resistance R_o, shunting the simulated collector current source, is rarely measured or applicable to large-signal stage design. It is present symbolically in the equivalent circuit solely to acknowledge that a finite parallel output resistance exists.

This equivalent circuit becomes a powerful tool in the design of broad-band large-signal output-matching circuits. The constraints for designing the output-matching circuit can be easily described if one views the true transistor collector as point C' in the equivalent circuit. In working from this point towards the load, the first two elements in the output-matching network will be the capacitance C_o, which is a fixed element in the network, and L_o, which is the minimum value of series collector lead inductance. In adding any circuitry external to the transistor package, L_o is a variable circuit element which can be increased beyond its minimum value by extension of the external collector lead. The remainder of the output-matching circuit remains to be completed using a topology that affords good bandwidth potential.

The design constraints for the output-matching circuit can be simply described in terms of an admittance at C', the internal collector node. Referring to Fig. 3, this admittance is represented by Y_L', which is comprised of a conductance G and susceptance B. It has been found convenient to view this admittance as comprised of a parallel combination of a resistance $R_p = 1/G$ and a reactance $X_p = -1/B$. The parallel resistance R_p is the resistive load line which relates to the power output level desired principally as a function of the collector dc supply voltage V_{cc}.

There are several oversimplified design expressions in the field of large-signal amplifiers. The results from these expressions are sufficiently inconsistent to warrant their being referred to as myths. One such myth is the expression $R_L \approx V_{cc}^2/2P_o$, where R_L is the parallel resistive load line synonymous with R_p; V_{cc} is the dc collector supply voltage; and P_o is the desired output power. Basic frequency-dependent factors not considered in this expression are collector voltage and current waveforms and their phasing, conduction angle, and the collector RF saturation voltage. It is probably impractical to pursue the analytic description of these factors in any expression.

General experience with large-signal devices has given insight to a rather simple behavior pattern for R_p. As a meaningful point of reference, one can relate to the value of R_p for which the transistor can produce its rated output power. Assuming V_{cc} is held fixed, there is an approximately fixed value of R_p for which the transistor will produce its rated output power over its usable frequency range. For example, the MSC 2010 is rated to produce 20 W of output power at frequencies of 1 GHz and below, approximately 15 W at 1.5 GHz and 10 W at 2 GHz. To realize this rated output power, the value of R_p is constant at 20 Ω at all frequencies. Furthermore, this value of R_p is correct for every available 10-W, 2-GHz transistor from all manufacturers.

This observation has been repeatedly confirmed by load-pull data and manufacturer's data translated to the node C' in the equivalent circuit. For example, if one takes the manufacturer's collector load impedance data which corresponds to Z_{CL} for the MSC 2010 at its rated output power and then translates it back through the equivalent value of L_o of 1.2 nH and C_o of 10 pF, the impedance at C' is very close to $20+j0$ Ω at frequencies of 1.0, 1.5, and 2.0 GHz.

At a given frequency it should be noted that at power levels below rated power the approximately correct value of R_p varies inversely with power output. Therefore, to assure near-constant saturated output power with frequency, the value of R_p must decrease directly with frequency. For 10-W output from the transistor mentioned, R_p varies linearly from 40 Ω at 1 GHz to 20 Ω at 2 GHz. In many cases, this R_p behavior over broad bandwidths cannot be readily simulated.

In most design situations, a reasonable constraint for the load-line resistance at C' is to maintain R_p at a fixed nominal value over the band within some acceptable tolerance. Excellent broad-band designs have been repeatedly achieved by assuming an R_p constrained to an allowable deviation of ± 10 percent from a nominal value over the band.

The transistor collector efficiency should be optimal when the capacitance C_o is tuned out leaving a purely resistive load line R_p. This optimal tuning, while attainable at one or more frequencies in the band, is a physical impossibility to provide continuously over the band. The greater the degree of detuning, the lower the value of X_p and the greater the sacrifice in collector efficiency from the maximum achievable value. Therefore, to assure adequate collector efficiency, a means of describing a minimum acceptable X_p is necessary as a design constraint. Excellent efficiency has been consistently achieved by imposing the following constraint upon X_p: Within the operating band, the magnitude of X_p at any frequency must be not less than twice the value of $R_p(|X_p|/R_p \geq 2)$.

Situations arise where a design for the desired bandwidth cannot be generated when adhering to these constraints. Bandwidth can be extended at a sacrifice in collector efficiency by loosening the constraint on X_p. Acceptable results have been realized using $|X_p|/R_p \geq 1$ in several instances. Increasing the allowable deviation of R_p from its nominal value represents an additional means to reach a compromise between performance and bandwidth.

The Output-Matching Network

A continuing evaluation of potential topologies for broad-band output-matching networks has revealed the all low-pass-type structure to be the most practical topology for broad-band implementation. Fig. 4 schematically represents a low-pass structure in lumped-element form. The output equivalent circuit of an MSC 2010 transistor with C_o of 10 pF and L_o of 0.8 nH is included in the network. This circuit is an optimal design for $18 \leq R_p \leq 22$ Ω and a $|X_p|/R_p \geq 2$. These constraints are satisfied over a bandwidth from 1030 to 1450 MHz. Fig. 5 depicts, through shading on a Smith chart, the impedance region bounded by these constraints together with the calculated frequency locus of $1/Y_L'$ for the circuit. At a point just outside the transistor package corresponding to node X in the schematic, the calculated driving point impedance Z_x is also indicated. The real component of Z_x varies from 4.5 to 7.0 Ω. This has ramifications to be discussed later. Fig. 6 shows the measured collector efficiency of the transistor as a function of frequency with output power held to a constant 13-W CW over the band. Although not evident from this figure, saturated output power was a maximum of 18 W at 1050 MHz tapering to 13 W at 1450 MHz. The acceptable measured bandwidth is shown to be from 1010 to 1460 MHz,

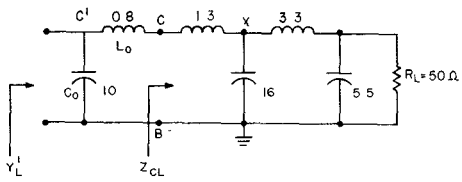

Fig. 4. A lumped-element broad-band output-matching circuit which meets the design constraints of $18 \leq R_p \leq 22\ \Omega$ and $|X_p|/R_p \geq 2$ from 1030 to 1450 MHz. Values in picofarads and nanohenrys.

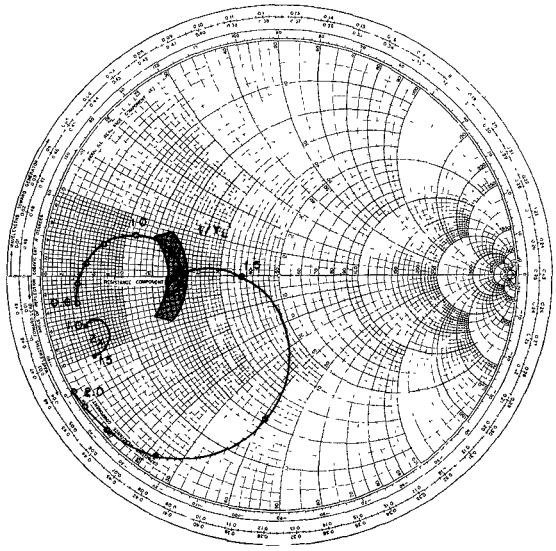

Fig. 5. Driving-point impedances with frequency for the circuit of Fig. 4. Frequency in gigahertz. 0.1-GHz intervals.

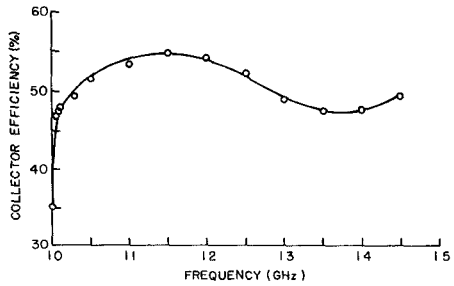

Fig. 6. A plot of measured collector efficiency versus frequency for the design of Fig. 4 at a constant output power of 13 W. $V_{cc} = 28$ V. $P_{out} = 13$ W.

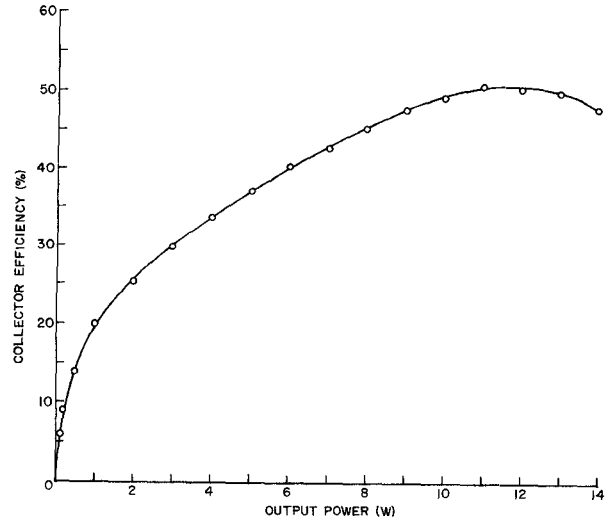

Fig. 7. The typical behavior of collector efficiency with output power varied through input drive for a common-base transistor stage. $V_{cc} = 28$ V.

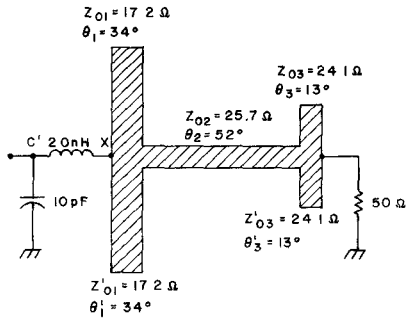

Fig. 8. A distributed circuit which has the equivalent driving-point impedance as the lumped-element circuit of Fig. 4. θ is the length at 1 GHz. All stubs are open circuited.

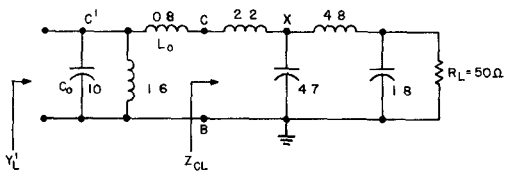

Fig. 9. A lumped-element output circuit employing the INSHIN. Design constraints of $18 \leq R_p \leq 22\ \Omega$ and $|X_p|/R_p \geq 2$ over the frequency range of 1080 to 1860 MHz. Values in picofarads and nanohenrys.

exceeding by 30 MHz the calculated band conforming to the design constraints. Below 1010 MHz, the collector efficiency drops off abruptly to about 35 percent at 1000 MHz. At 1500 MHz, the load line appears nearly real with $R_p = 40\ \Omega$. Saturated output power is 6 W at 53-percent collector efficiency.

Fig. 7 depicts the behavior of efficiency with output power for this common base power stage at 1450 MHz. Output power was varied through input drive adjustment.

This circuit was originally fabricated using semilumped elements in microstrip [6]. A fully distributed-element low-pass topology was also optimized. The driving-point impedance with frequency for this circuit differs imperceptively from the lumped-element counterpart. Fig. 8 gives the distributed circuit element values combined with the lumped-equivalent output representation for the transistor. The circuit was fabricated using microstrip transmission lines of etched gold on 25-mil alumina substrates. Of more than ten broad-band stages constructed using this circuit, essentially identical broad-band performance has been achieved in each instance.

A startling increase in transistor bandwidth capability can be realized through the addition of an inductor which intimately parallels the transistor output capacitance. This intimacy requires fabricating the shunt inductor (together with a series capacitor to block the dc supply from ground) internal to the transistor package. In most situations, the shunt inductor is totally ineffective for bandwidth extension when it is positioned external to the transistor package.

Fig. 9 illustrates an optimal internal shunt inductor (INSHIN) lumped-element design for the MSC 2010. The previously imposed bandwidth design constraints of $18 \leq R_p$

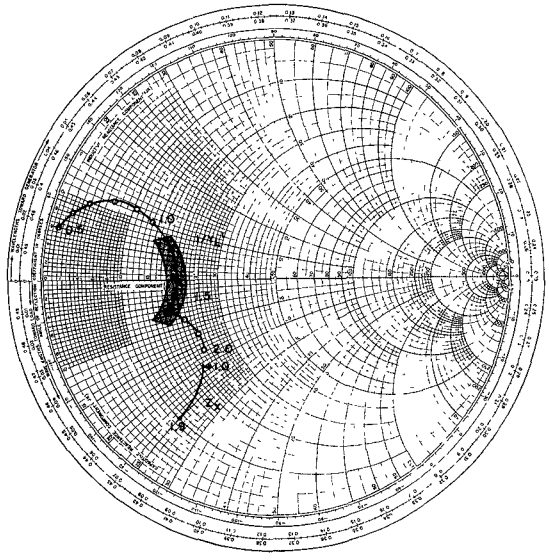

Fig. 10. Driving-point impedances with frequency for the INSHIN circuit of Fig. 9. Frequency in gigahertz. 0.1-GHz intervals.

$\leq 22\ \Omega$ and $|X_p|/R_p \geq 2$ are satisfied from 1080 to 1860 MHz. Broad-band performance has not been verified through measurements because of the unavailability of an MSC 2010 with an INSHIN.

Fig. 10 shows the frequency behavior of the impedance $1/Y_L'$ and the impedance Z_x. Some important observations, aside from bandwidth improvement, can be made in comparing the INSHIN circuit with the conventional low-pass network. The locus of $1/Y_L'$ indicates more effective utilization of the immittance region bounded by the design constraints. The impedance Z_x has a minimum series real component of $10\ \Omega$ at 1900 MHz as compared to $4.5\ \Omega$ minimum for the previous circuit. This higher resistive component of Z_x, being less sensitive to variations in the series inductance from C' to node X, permits the broad-band performance of these stages to be more easily reproduced. Without the INSHIN, this series inductance is the most sensitive circuit element in matching over a broad bandwidth. The higher impedance level lowers the ohmic power loss in the output-matching circuitry, since current levels at this point for a particular power output are lower.

With reference to the two schematic representations of Figs. 4 and 9, it is apparent that much smaller shunt capacitors are used in the INSHIN circuit, particularly at node X where only 4.7 pF is required as contrasted to 16 pF. When constructed in semilumped-element microstrip, this results in significantly smaller overall circuit area. Furthermore, the INSHIN output circuit will be of lower loss as the smaller value capacitors will have higher Q values than larger value capacitors. The foregoing factors become more significant for larger output capacitance (i.e., higher power level) transistors in this frequency range or alternately for a transistor with a given output capacitance operating at higher frequencies.

One additional factor affecting collector efficiency, particularly notable at frequencies above 2 GHz, should be mentioned. The transistor has an output Q given by $Q = 2\pi f R_p C_o$. Reactive stored energy J_r is related to delivered energy J_o in the following way: $J_r = QJ_o/2\pi$. As output Q increases, the ratio of reactive energy to delivered energy increases. Without the INSHIN, this reactive energy must flow principally through L_o, then through the large shunt capacitor at node X, and return through ground. The reactive energy encounters whatever losses exist in this path. The reactive energy lost must be replaced during every cycle in order for steady-state operation to be maintained. A portion of the fundamental frequency RF energy developed by the transistor, that would otherwise be available for delivery to the load, must be sacrificed to replace the dissipated reactive energy. With the INSHIN employed, the reactive energy flow is principally contained in the short part of the parallel tank circuit comprised of the INSHIN and C_o. The losses in reactive energy are thereby lowered accordingly. The higher the frequency and/or the higher the transistor output power, the more pronounced the improvements attributable to the INSHIN.

There is a general guideline in choosing good design values for the shunt inductor; it should resonate with the output capacitance in the lower portion of the band of interest. Typically, one-fifth of the bandwidth from the lower band edge gives the best broad-band results. Resonating towards the upper band edge yields less bandwidth and contributes to operating instabilities in the lower portion of the band.

Although the most ostensible contribution from the INSHIN over a conventionally packaged transistor is bandwidth extension, the important contributions of the INSHIN to moderate bandwidth applications which are within the capability of a conventionally packaged transistor should be delineated.

1) The collector load line is much less sensitive to variations in the collector series lead inductance. These variations result from mechanical tolerances in the transistor package and at the interface between the package and the external output-matching circuitry. This sensitivity with conventionally mounted transistors is a principal production obstacle to ready reproducibility of broad-band performance.

2) The INSHIN permits the use of smaller, simpler, lower loss, output-matching networks. The principal advantage at lower frequencies (below about 2.5 GHz) is the smaller size of microstrip circuitry needed. Circuit area will be reduced from one-half to two-thirds over the conventionally packaged transistor.

3) The INSHIN permits smaller sacrifices from the maximum tuned value of collector efficiency over the operating band.

4) For transistors operating at 3 GHz and above, the INSHIN will permit achieving a greater rated output power and higher tuned collector efficiency.

The authors had established the above claims and openly presented them to manufacturers of microwave transistors as early as August 1970. It was recently learned that Belohoubek and colleagues had suggested the INSHIN for the purpose of broadening bandwidth and improving stability of power transistors in a contract proposal to develop a broad-band transistor power amplifier [6]. The first implementations of the INSHIN known to the authors were made independently by Caulton *et al.* [7] and by Belohoubek *et al.* [1]–[3]. Both groups were working to develop microwave power-transistor chip carriers as a means to minimize the parasitic deficiencies present in conventional transistor packages.

Caulton used the INSHIN because an approximately 50-Ω value of R_p was needed. This simple inductor resonating C_o at the frequency of interest offered the simplest lowest loss circuit for matching the transistor to a 50-Ω load termination. Caulton did not investigate or describe any potential of bandwidth enhancement from the INSHIN.

Belohoubek successfully achieved octave bandwidth from 1 to 2 GHz with high-power transistors operating class A by employing the INSHIN as part of sophisticated transistor chip carriers [3]. In this work, the stability and bandwidth enhancement of the INSHIN was verified. With respect to stability, [3] describes important factors relevant to the proper fabrication of the INSHIN.

The first commercially available transistor to incorporate the INSHIN was introduced by Power Hybrids, Inc., in 1972. The manufacturer acknowledged the claims of improved efficiency over moderate bandwidths and reduced difficulty in output matching [8].

More recently, the INSHIN has demonstrated the validity of the foregoing claims on four Government contracts [9]–[12] from the U. S. Army Electronics Command (Fort Monmouth, N. J.) sponsored by the U. S. Army Advanced Ballistic Missile Defense Agency. The contracts are related to the development of L- and S-band power transistor chip carriers and S-band phased-array radar transistor power amplifiers.

Broad-Banding Limitation of Large-Signal Transistor Output Circuits

The subject of broad-banding limitations as they apply to simple nonreal terminations has been analytically described by Bode [13]. Bode's work has been successfully applied to provide fundamental guidelines for the design of impedance-matching filters and networks [14], [15]. Broad-band circulator matching networks have been synthesized based on Bode's work [16]. If one is to apply Bode's work to broad-band large-signal transistor matching, one must be aware of the differences in the transistor design constraints from those used in synthesizing networks for general matching problems.

Bode described the conservation of bandwidth in terms of the integral of reflection coefficient with frequency [13].

$$\int_0^\infty \log \left|\frac{1}{\rho}\right| d\omega = \frac{\pi}{RC} .$$

This expression applies to any lossless minimum reactance network terminated in a simple parallel combination of resistance R and capacitance C. The network reflection coefficient is ρ. If one constrains the behavior of ρ so that $|\rho| < 1$ within some prescribed frequency range from ω_1 to ω_2 and $|\rho| = 1$ everywhere outside the band, the expression is simplified to be

$$\int_{\omega_1}^{\omega_2} \log \left|\frac{1}{\rho}\right| d\omega = \frac{\pi}{RC} .$$

This relationship is useful in problems dealing with a conventional driving source, where power transfer is best observed by a nominal internal impedance which is conjugately matched. The internal source impedance (or output impedance) of a class-C transistor is nonlinear and unpredictable. Therefore, descriptions involving reflection coefficients are not meaningful.

A more suitable means for assessing bandwidth capability for transistors is available through the Bode resistance integral (or attenuation integral) theorem [13]—a corollary to the integral based upon reflection coefficient.

Given any minimum reactance network where the leading element at the input to the network is a shunt capacitor C and where the input impedance of the network has a finite-series real component R, the following integral applies:

$$\int_0^\infty R\, d\omega = \frac{\pi}{2C} .$$

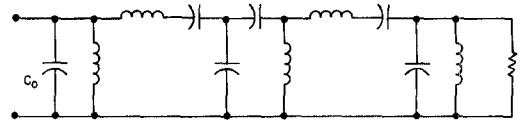

Fig. 11. A fully bandpass topology including an ideal transformer.

This theorem can be most simply summarized for broad-bandwidth large-signal transistor applications as follows. To best conserve the ultimate power-bandwidth capability of a transistor within a frequency range for which it is a useful active device, a network should be designed such that an appropriate load-line resistance be realized at the transistor's internal collector terminal to satisfy the power-output objectives over the operating bandwidth. The ultimate operating bandwidth will be realized if, at all frequencies outside the operating band, the series resistance seen at the internal collector terminal is zero.

In view of meeting this attitude on resistance behavior, the ultimate network would be of a true bandpass variety and provide very abrupt transition to zero resistance outside the useful operating range. Fig. 11 illustrates a bandpass circuit accommodating these goals using discrete lumped-element construction. Since impedance transformation is a frequent necessity, ideal transformers in lumped form must be incorporated into the structure [14]–[17]. The odd capacitor in this structure results from incorporating an ideal transformer.

The realization of the ultimate bandwidth capability with lossless reactive elements requires an infinite number of reactive elements. Best approximation to the ultimate bandwidth assumes the synthesis of elliptic function networks. A Chebyshev-type network is normally considered for simplicity in synthesis and physical construction with only a small loss in bandwidth.

While true bandpass matching sections offer the broadest bandwidth capability, there are practical considerations which limit their usefulness. For a given number of circuit arms, there are twice as many circuit elements in the bandpass structure as there are in the low-pass or high-pass structures. Secondly, conventional bandpass design based upon the classic low-pass-to-bandpass transformation frequently results in unacceptable element values for practical implementation.

Figs. 12 and 13 allow a graphical assessment of the broad-band utilization of the structures discussed previously. All designs relate to a 10-pF value of C_o which means $\pi/2C = 1.57 \times 10^{11}\ \Omega \cdot \text{rad/s}$. Therefore, the constant resistance integral can be rewritten for this case:

$$\int_0^\infty R\, d\omega = 1.57 \times 10^{11}\ \Omega \cdot \text{rad/s}.$$

There is one point to be clarified. The networks were designed as previously described to maintain R_p, the parallel resistance at C', nearly constant with frequency. Regardless of this design attitude, in applying the Bode integral in the form indicated, one considers the equivalent series resistance of the network at C' for bandwidth assessment.

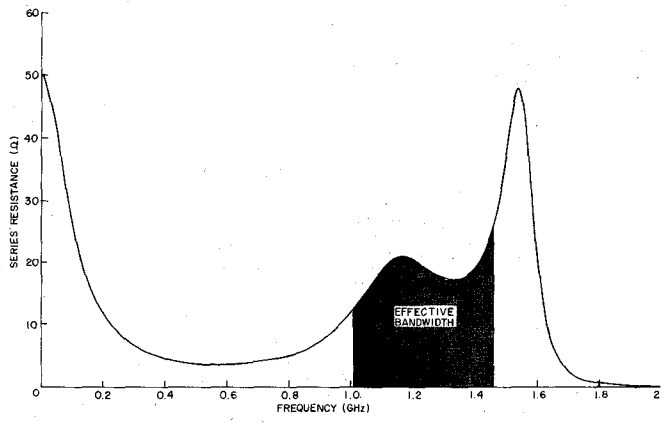

Fig. 12. A plot of series input resistance at the internal collector node C' with frequency for the circuit of Fig. 4.

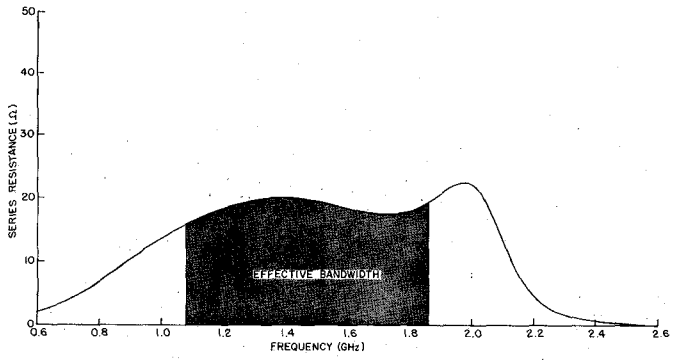

Fig. 13. A plot of series input resistance at the internal collector node C' with frequency for the INSHIN circuit of Fig. 9.

Fig. 12 is a plot of series input resistance at C' for the circuit of Fig. 4. By integrating under this curve, the value of 1.57×10^{11} Ω·rad/s was confirmed within 0.1 percent. Since this circuit effectively met good broad-band performance from 1010 to 1460 MHz, the resistance integral taken over this band represents the effectively utilized portion of the potentially available bandwidth. Integrating over this bandwidth gives a value of 0.531×10^{11} Ω·rad/s. This is 33.6 percent of the total integral taken for ω over the span from zero to ∞. This result suggests that if the total bandwidth potential were utilized within the formerly applied design constraints, about 1350 MHz of potential bandwidth is available. To approach this would require a very complex, impractical network.

Fig. 13 represents the behavior of the INSHIN design of Fig. 9, which has a bandwidth defined from 1080 to 1860 MHz. Integrating the series resistance apparent at C' over this bandwidth gives a value of 0.912×10^{11} Ω·rad/s. This represents 58 percent of the potentially available value of 1.57×10^{11} Ω·rad/s.

These curves give a meaningful understanding of where bandwidth is wasted. For the INSHIN circuit, no bandwidth potential is sacrificed below 500 MHz, and there is only a moderate loss outside the upper edge of the band. On the other hand, the conventional low-pass circuit without the INSHIN sacrifices 0.50×10^{11} Ω·rad/s below 500 MHz and has a much greater peak outside the upper band edge. The bandpass characteristic achieved by the INSHIN below the lower edge of the band is principally responsible for the additional bandwidth realized.

The Input-Matching Circuit

The input-matching circuit is responsible for achieving level gain over the operating bandwidth. Large-signal microwave transistors exhibit a notable change in input characteristics as a function of collector-loading changes. The collector loading, on the other hand, can be designed independently to satisfy power-output and collector-efficiency considerations. A pragmatic approach to the design of an overall stage is to determine a suitable output-matching network first, then design the input-matching section to satisfy one's gain requirements.

At microwave frequencies, the transistor input of large-signal transistors can be closely represented by a real component, often 1 Ω or less, in series with an inductive component. For common-base stages, both the real and the inductive components demonstrate moderately increasing values with frequency.

The most promising topology for input matching consists of a two-section low-pass impedance-transforming structure which nicely absorbs the series RL nature of the transistor. The low-pass structure which employs shunt capacitors is also more readily constructed in microstrip than a high-pass or bandpass structure, which would require series capacitors in their realization.

The philosophy for the input-matching circuit hinges upon the transistor's power gain falloff versus frequency. One attempts to find a network which closely matches the transistor to the source impedance, typically 50 Ω, at the uppermost frequency in the band. At this frequency, transistor power gain will be lowest and close matching will avoid gain sacrifices. At lower frequencies, power gain is greater but must be sacrificed to achieve gain leveling. There are no practical means to construct dissipative networks tailored to complement the transistor's gain–frequency behavior. Gain compensation through reflective attenuation of input power is a practical alternative. The network can be realized in the low-pass form using low-loss elements in microstrip. Tables of lumped-element designs for networks of this form exist [18]. While these tables can be quite effectively applied to the input matching of common-emitter stages at frequencies below 1 GHz, they best serve only as a rough guide for designing at higher frequencies.

Because of the interrelationship between collector loading and gain at microwave frequencies, one cannot assume the classic 6-dB/octave gain rolloff nor a constant gain slope with frequency. Similarly, the input impedance is a function of collector loading.

The design of the input circuit can be developed using computer-aided techniques once the appropriate characterization data are available.

With the transistor operating at the objective output power with the selected output-matching network, the input impedance and the input drive power are measured over the desired frequency band. These drive power and input impedance data can be utilized to computer-design the input-matching structure so that the appropriate reflective attenuation with frequency for level gain over the band will be approximated. A fixed incident power from a constant generator impedance is assumed in the computer design. In practice, such a source would be implemented by use of a 3-dB quadrature hybrid feeding a balanced pair of stages.

Some pertinent points may be made regarding the input characterization and circuit realization. The series input resistance of most large-signal transistors is quite low. It is most

difficult to measure as precisely as one desires for characterization. Secondly, the series input Q of the transistor will be high. This Q may be greater than ten in many cases. The transistor input Q is given by:

$$Q = \frac{\omega L_{in}}{R_{in}}$$

where ω is some radian frequency in the band, L_{in} is the series input inductance series specified at ω. The low-pass input-matching circuit will require a large capacitor shunting the transistor input at a point as close to the package as possible. In many cases, the Q of the capacitor may be only five times the series input Q of the transistor. This would contribute a 1-dB loss in drive power. This loss would have to be represented in the low-pass computer-design simulation. If not, the fabricated input-matching circuit performance will depart grossly from the intended performance of the computed design.

There is a practical input characterization which inherently includes the above error considerations. One characterizes the transistor together with a known value of input capacitor which is anticipated to be the appropriate value. With moderate experience, one can estimate the proper capacitance within 20 percent of the final design value. Fig. 14 shows such a characterization for a 10-W 2-GHz transistor using a 10-pF shunt capacitor butted snugly to the package input. In an optimal-seeking computer design, one can simulate a lossless capacitor immediately paralleling the characterization impedance. Minor capacitance value changes will not cause Q value changes of any consequence. The program may be made to adapt to negative capacitance values as well. For example, assume the optimum shunt capacitance to be 9 pF while characterization is made with 10 pF. The computer design would indicate a -1.0-pF capacitor being added to realize a 9-pF value.

The characterization of Fig. 14 evidences some disturbing facts about bandwidth potential with respect to gain leveling of the input. The input Q is so large in the frequency band that the transistor series input resistance is transformed to 150-Ω real at 1.3 GHz with the shunt capacitor introduced. One normally intends to transform to a nominal 50-Ω impedance level using a two-section matching network, if the input is to be driven from conventional 3-dB quadrature hybrids. Once the first section has transformed the input to a resistance greater than 50 Ω, the second section can give gain leveling over a small bandwidth. For this transistor, level gain was realizable over only 300 MHz from 1100 to 1400 MHz and this at the expense of a 2-dB gain sacrifice to 6 dB from the input-matched gain value of 8 dB at 1400 MHz.

The difficulties noted are quite apparent with all of the higher power transistors in use. The highest power transistors available are extremely difficult to match over bandwidths greater than 100 MHz. Furthermore, the capacitor directly shunting the transistor input generally represents a large value which consumes an inordinate area if fabricated as a microstrip structure. Smaller, lumped-element capacitors with acceptable Q values are not commercially available.

The advent of internally matched transistor inputs is the solution to many input-matching limitations. Input-matching networks of the two-section low-pass type are fabricated using lumped-element capacitors of metal–oxide–silicon or metal–oxide–metal construction. Inductors are realized through

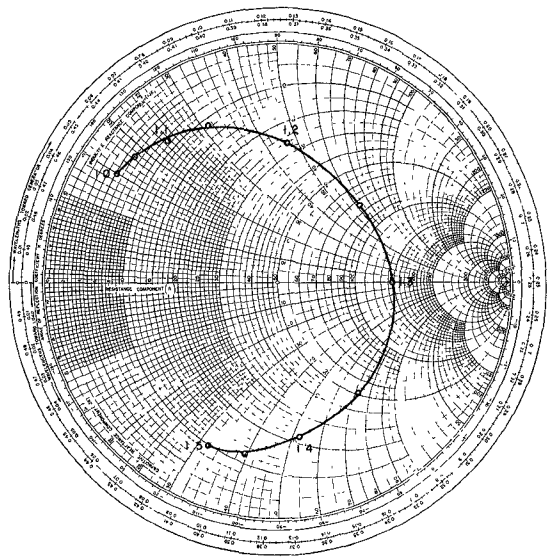

Fig. 14. Input impedance with frequency for a common-base transistor with the input shunted by a 10-pF capacitor. Frequency in gigahertz.

lengths of 1- or 2-mil-diameter bond wire. The first matching section can be realized with a very low Q (from 2 to 5 is typical). At the package input to the internally matched transistor, the most desirable impedance level would consist of a series real part in the range of 20–35 Ω in the band of interest. The final matching to 50 Ω is accomplished simply, external to the package. Such external matching permits the designer flexibility in adapting the input match to other than a single custom band. Also, some phase and amplitude characteristics of pulses can be predominantly tailored through this final input match. Experience has indicated that the desired broad-band gain leveling of internally matched transistors over broad bandwidths can be accomplished readily with empirical tuning. As such, careful characterization and computer-aided design is unnecessary.

Conclusions

Practical approaches for the characterization of large-signal microwave transistors have been described. Several useful topologies, effective for realizing broad-band transistor-matching networks, were suggested. Specific design constraints, particularly valuable in the computer-aided design of broad-band matching networks, were presented and discussed. Using one of the characterization approaches together with the design constraints resulted in a transistor stage with a minimum output power of 13 W from 1010 to 1460 MHz and minimum collector efficiency of 47 percent in this band. The merits of an inductor shunting the transistor collector internal to the package was fully explored as a practical means for extending broad-band performance. A circuit design which should permit extending the previous 450-MHz bandwidth to 780 MHz illustrated the potential of this internal inductor. The use of the Bode constant-resistance integral theorem was demonstrated as a means for quantitatively examining the ultimate bandwidth potential of large-signal transistors and the bandwidth utilization of specific circuit designs.

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They wish to thank V. Garboushian of Power Hybrids, Inc., for his early initiative in implementing the internal shunt inductor and acknowledging its potential as a broadband matching element in response to our suggestion.

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Characteristics of IMPATT-Diode Reflection Amplifiers

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***Abstract*—The results of an investigation of the gain, stability, phase shift, power addition, saturation, and bandwidth properties of microwave reflection amplifiers which employ IMPATT diodes as the active element, together with the dependence of all these properties upon the device material, doping profile, and operating conditions, are presented. Both Si and GaAs diodes are considered and experimental results demonstrating the validity of the model are provided, together with other experimentally determined characteristics relating gain, saturation, and bandwidth to current density and tuning conditions. Finally, measurements illustrating the degradation of response as a result of subharmonic oscillation are given.**

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I. Introduction

STABLE reflection gain from an amplifier utilizing an IMPATT diode as the active device was first reported by Napoli and Ikola in 1965 [1]. Subsequently, significant advances have been made in power output [2], operating frequency [3], and gain-bandwidth optimization [4], and several analytical techniques for the design of amplifiers of this type have been described [5]–[8]. These techniques, however, all rely on either experimentally determined device immittance data or on Read [9] model theory, and therefore do not address the problem of optimization of device properties for stable reflection amplifiers.

The purpose of this paper is to provide an improved understanding of the design and analysis of microwave reflection amplifiers employing the negative-resistance property of IMPATT diodes, to demonstrate the validity of that theory by means of experiment and, finally, to utilize the theory to examine the properties of such amplifiers and the dependence